IN THE CLAIMS

1. (Currently Amended) For use with network systems that employ packets having an associated priority, a head of line blockage avoidance system, comprising:

m inputs, m numbering at least two, configured to receive said packets;

n packet first-in-first-out buffers (FIFOs), n numbering at least two, each of said n packet FIFOs occupying a same hierarchical level and configured to receive at least one of said packets from said m inputs, said n packet FIFOs configured as m subsets of packet FIFOs, each of said packet FIFOs in each of said subsets being coupled to a different one of said m inputs;

a priority summarizer configured to generate a priority summary of said packets within said m inputs and said n packet FIFOs that indicates which of said n packet FIFOs is to receive a highest priority packet from one of said m inputs, wherein each of said n packet FIFOs can receive packets of two or more differing priorities; ~~and~~

a scheduler configured to cause packets in said n packet FIFOs to be queued for processing based on said priority summary such that packets in a packet FIFO that is to receive said highest priority packets are triggered to be processed before packets in other of said n packet FIFOs so that a lower priority packet in said n packet FIFO is scheduled for processing before a higher priority packet concurrently contained in another of said n packet FIFOs is scheduled for processing; and

a destination FIFO and an output, said destination FIFO interposing said n packet FIFOs and said output, said scheduler further configured to transfer at least one of said packets from one

of said m inputs toward said output only if said n packet FIFO and said destination FIFO are both available to simultaneously contain said packet.

2. (Canceled)

3. (Previously Presented) The head of line blockage avoidance system as recited in Claim 1 wherein said priority summary further indicates an order in which to transmit said at least one of said packets contained within said n packet FIFOs to a destination FIFO based upon packet priority.

4. (Previously Presented) The head of line blockage avoidance system as recited in Claim 1 wherein each of said m inputs includes a source FIFO configured to contain at least one of said packets.

5. (Previously Presented) The head of line blockage avoidance system as recited in Claim 4 wherein said priority summarizer is further configured to generate said priority summary of said packets within each of said n packet FIFOs and said packets within said source FIFO of each of said m inputs that are to be transferred to said each of said n packet FIFOs.

6. (Canceled)

7. (Previously Presented) The head of line blockage avoidance system as recited in Claim 1 wherein said scheduler is further configured to assign said associated priority to each of said packets based on a priority associated with each of said m inputs or a destination.

8. (Currently Amended) For use with network systems that employ packets having an associated priority, a method of operating a head of line blockage avoidance system, comprising:

employing m inputs, m numbering at least two, configured to receive said packets;

employing n packet first-in-first-out buffers (FIFOs), n numbering at least three, each of said n packet FIFOs occupying a same hierarchical level and configured to receive at least one of said packets from said m inputs, said n packet FIFOs configured as m subsets of packet FIFOs, each of said packet FIFOs in each of said subsets being coupled to a different one of said m inputs;

generating a priority summary of said packets within said m inputs and said n packet FIFOs that indicates which of said n packet FIFOs is to receive a highest priority packet from one of said m inputs, wherein each of said n packet FIFOs can each receive packets of two or more priorities; and

scheduling packets in said n packet FIFOs to be processed based on said priority summary such that packets in a packet FIFO that is to receive said highest priority packets are triggered to be processed before packets in other of said n packet FIFOs so that a lower priority packet in said n packet FIFO is scheduled for processing before a higher priority packet concurrently contained in another of said n packet FIFOs is scheduled for processing,

wherein said scheduling further causes a packet to be transmitted from one of said m inputs

toward an output only when both said n packet FIFO, selected to receive said packet, and an interposing destination FIFO, coupled to a plurality of said n packet FIFOs, only if said n packet FIFO that is selected to receive said packet and said destination FIFO are both available to simultaneously contain said packet.

9. (Canceled)

10. (Previously Presented) The method as recited in Claim 8 wherein said priority summary further indicates an order in which to transmit said at least one of said packets contained within said n packet FIFOs to a destination FIFO based upon packet priority.

11. (Previously Presented) The method as recited in Claim 8 wherein each of said m inputs includes a source FIFO configured to contain at least one of said packets.

12. (Previously Presented) The method as recited in Claim 11 wherein said generating further comprises generating said priority summary of said packets within each of said n packet FIFOs and said packets within said source FIFO of each of said m inputs that are to be transferred to said each of said n packet FIFOs.

13. (Canceled)

14. (Previously Presented) The method as recited in Claim 8 wherein said scheduling further comprises assigning said associated priority to each of said packets based on a priority associated with each of said m inputs or a destination.

15. (Currently Amended) A crossbar head of line blockage avoidance system that employs packets having an associated priority, comprising:

m physical interfaces, m numbering at least two;

m inputs, each of said inputs coupled to corresponding ones of said m physical interfaces to receive said packets;

m outputs that transmit said packet to corresponding ones of said m physical interfaces, each of said outputs having:

n packet first-in-first-out buffers (FIFOs), n numbering at least m, each of said n packet FIFOs occupying a same hierarchical level and configured to receive at least one of said packets from said m inputs, said n packet FIFOs configured as m subsets of packet FIFOs, each of said packet FIFOs in each of said subsets being coupled to a different one of said m inputs, and

a destination FIFO interposing said n packet FIFOs and said output;

a priority summarizer that generates a priority summary of said packets within said m inputs and said n packet FIFOs within each of said m outputs that indicates which of said n packet FIFOs is to receive a highest priority packet from one of said m inputs, wherein said n packet FIFOs can each receive packets of two or more priorities; and

a scheduler that causes packets in said n packet FIFOs for each of said m outputs to be queued for processing based on said priority summary such that packets in a packet FIFO that is to receive said highest priority packets are triggered to be processed before packets in other of said n packet FIFOs so that a lower priority packet in said n packet FIFO is scheduled for processing before a higher priority packet concurrently contained in another of said n packet FIFOs is scheduled for processing; and

a destination FIFO and an output, said destination FIFO interposing said n packet FIFOs and said output, said scheduler further configured to transfer at least one of said packets from said one of said inputs toward said output only if said n packet FIFO and said destination FIFO are both available to simultaneously contain said packet.

16. (Canceled)

17. (Previously Presented) The crossbar head of line blockage avoidance system as recited in Claim 15 wherein said priority summary further indicates an order in which to process said n packet FIFOs for each of said m outputs based upon packet priority.

18. (Previously Presented) The crossbar head of line blockage avoidance system as recited in Claim 15 wherein each of said m inputs includes a source FIFO configured to contain at least one of said packets.

19. (Previously Presented) The crossbar head of line blockage avoidance system as recited in Claim 18 wherein said priority summarizer generates said priority summary of said packets within each of said n packet FIFOs and said packets within said source FIFO of each of said m inputs that are to be transferred to said each of said n packet FIFOs.

20. (Cancelled)

21. (Previously Presented) The head line block system of Claim 1, further comprising:

wherein said priority summarizer is further configured to generate a priority summary of said packets within said m inputs and said n packet FIFOs that indicates which of said n packet FIFOs either contains or is to receive a highest priority packet from one of said m inputs; and

wherein said scheduler is further configured to cause packets in said n packet FIFOs to be queued for processing based on said priority summary such that packets in a packet FIFO that either contains or is to receive said highest priority packets are triggered to be processed before packets in other of said n packet FIFOs.

22. (Previously Presented) The method of Claim 8, further comprising:

generating a priority summary of said packets within said m inputs and said n packet FIFOs that indicates which of said n packet FIFOs either contains or is to receive a highest priority packet from one of said m inputs; and

scheduling packets in said n packet FIFOs to be processed based on said priority summary

such that packets in a packet FIFO that either contains or is to receive said highest priority packets are triggered to be processed before packets in other of said n packet FIFOs.

23. (Previously Presented) The system of Claim 15, further comprising:

wherein said priority summarizer is configured to generate a priority summary of said packets within said m inputs and said n packet FIFOs that indicates which of said n packet FIFOs either contains or is to receive a highest priority packet from one of said m inputs; and

wherein said scheduler is further configured to cause packets in said n packet FIFOs to be queued for processing based on said priority summary such that packets in a packet FIFO that either contains or is to receive said highest priority packets are triggered to be processed before packets in other of said n packet FIFOs.